CLAIMS

What is claimed is:

1. A power efficient integrated circuit comprising:

phase lock loop operably coupled to receive a reference clock and to produce therefrom a system clock based on a system clock control signal;

on-chip power supply control module operably coupled to regulate at least one supply from a power source and an inductance based on a power supply control signal;

memory operably coupled to store at least one application; and

computational engine operably coupled to produce the system clock control signal and the power supply control signal based on a processing transfer characteristic of the computation engine and processing requirements associated with processing at least a portion of the at least one application.

2. The power efficient integrated circuit of claim 1, wherein each of the at least one application comprises the processing requirements for at least one of: each sub-routine contained in the application and the application.

3. The power efficient integrated circuit of claim 1, wherein the computational engine further comprises:

training module operably coupled to determine the processing transfer characteristic and the processing requirements based on a known executional requirements of a given function, wherein the known executional requirements includes at least one of: millions of instructions per second (MIPS), timing requirement between dependent operations, and speed of execution.

4. The power efficient integrated circuit of claim 3, wherein the given function further comprises at least one of: reading from memory, executing a test multiply-accumulate function, and propagating data through combinational logic circuit.

5. The power efficient integrated circuit of claim 4, wherein the training module further comprises:

system clock determining module operably coupled to determine a first system clock control signal based on MIPS required to complete the given function such that the system clock is set to a minimum frequency to met the MIPS required; and

power supply determining module operably coupled to increment the power supply control signal causing the at least one supply to be incrementally increased for each processing of the given function until the given function provides an anticipated result.

6. The power efficient integrated circuit of claim 1, wherein the phase lock loop further comprises:

at least one divider module; and

a register operably coupled to the at least one divider module, wherein the register stores various divider values that are selected based on the system clock control signal.

7. The power efficient integrated circuit of claim 1, wherein the on-chip power supply further comprises a programmable divider circuit that is programmed based on the power supply control signal.

8. The power efficient integrated circuit of claim 1, wherein the at least one supply further comprises multiple supplies that are produced from the system clock and multiple

power supply control signals, wherein each of the multiple power supply control signals corresponds to a unique one of the multiple supplies.

9. A method for controlling power consumption of an integrated circuit, the method comprises the steps of:

producing a system clock from a reference clock based on a system clock control signal;

regulating at least one supply from at least one of: a linear regulator and a power source and an inductance based on a power supply control signal; and

producing the system clock control signal and the power supply control signal based on a processing transfer characteristic of a computation engine and processing requirements associated with processing at least a portion of an application by the computation engine.

10. The method of claim 9 further comprises retrieving the processing requirements from the application.

11. The method of claim 9 further comprises:

determining the processing transfer characteristic and the processing requirements based on a known executional requirements of a given function, wherein the known executional requirements includes at least one of: millions of instructions per second (MIPS), timing relationship between dependent operations, and speed of execution.

12. The method of claim 11 further comprises:

determining a first system clock control signal based on MIPS required to complete the given function such that the system clock is set to a minimum frequency to met the MIPS required; and

incrementing the power supply control signal causing the at least one supply to be incrementally increased for each processing of the given function until the given function provides an anticipated result.

13. The method of claim 9, wherein the producing the system clock from a reference clock based on a system clock control signal further comprises:

accessing a register based on the system clock control signal to retrieve a selected divider setting; and

adjusting a divider setting of a dividing in a phase lock loop that produces the system clock based on the selected divider setting.

14. The method of claim 9, wherein the regulating at least one supply further comprises adjusting a programmable divider circuit of an on-chip power converter based on the power supply control signal.

15. The method of claim 9, wherein the regulating the at least one supply further comprises regulating multiple supplies from the system clock and multiple power supply control signals, wherein each of the multiple power supply control signals corresponds to a unique one of the multiple supplies.

16. An apparatus for controlling power consumption of an integrated circuit, the apparatus comprises:

a processing module; and

memory operably coupled to the processing module, wherein the memory includes operational instructions that cause the processing module to:

produce a system clock from a reference clock based on a system clock control signal;

regulate at least one supply from at least one of: a linear regulator and a power source and an inductance based on a power supply control signal; and

produce the system clock control signal and the power supply control signal based on a processing transfer characteristic of a computation engine and processing requirements associated with processing at least a portion of an application by the computation engine.

17. The apparatus of claim 16, wherein the memory further comprises operational instructions that cause the processing module to retrieve the processing requirements from the application.

18. The apparatus of claim 16, wherein the memory further comprises operational instructions that cause the processing module to:

determine the processing transfer characteristic and the processing requirements based on a known executional requirements of a given function, wherein the known executional requirements includes at least one of: millions of instructions per second (MIPS), timing relationship between dependent operations, and speed of execution.

19. The apparatus of claim 18, wherein the memory further comprises operational instructions that cause the processing module to:

determine a first system clock control signal based on MIPS required to complete the given function such that the system clock is set to a minimum frequency to met the MIPS required; and

increment the power supply control signal causing the at least one supply to be incrementally increased for each processing of the given function until the given function provides an anticipated result.

20. The apparatus of claim 16, wherein the memory further comprises operational instructions that cause the processing module to produce the system clock from a reference clock based on a system clock control signal by:

accessing a register based on the system clock control signal to retrieve a selected divider setting; and

adjusting a divider setting of a dividing in a phase lock loop that produces the system clock based on the selected divider setting.

21. The apparatus of claim 16, wherein the memory further comprises operational instructions that cause the processing module to regulate at least one supply by adjusting a programmable divider circuit of an on-chip power converter based on the power supply control signal.

22. The apparatus of claim 16, wherein the memory further comprises operational instructions that cause the processing module to regulate the at least one supply by regulating multiple supplies from the system clock and multiple power supply control

signals, wherein each of the multiple power supply control signals corresponds to a unique one of the multiple supplies.